We claim:

1. An assembly structure for a memory device, comprising:

a substrate having at least one fold line thereon, dividing the substrate into at least two sections;

a layer of memory materials fabricated on each of the at least two sections, each layer being disposed so that the layers of memory materials on sections adjacent to each other form an interface in which the memory materials are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the fold line.

2. The assembly structure recited in claim 1, wherein the fold line runs approximately down the center of a definable portion of the substrate.

3. The assembly structure recited in Claim 1, wherein at least one of the layers of memory materials forming each of the interfaces comprises semiconductor patterns.

4. The assembly structure recited in Claim 1, wherein at least one of the layers of memory materials forming each of the interfaces comprises conductor line patterns.

5. The assembly structure recited in claim 1, wherein the layers forming at least one of the interfaces combine to provide a plurality of conductors and semiconductor patterns.

6. The assembly structure recited in claim 1, wherein the fold line comprises a series of aligned perforations.

7. The assembly structure recited in claim 1 wherein the fold line comprises at least one indentation in the substrate.

8. The assembly structure recited in claim 1 wherein the fold line comprises at least one crease in the substrate..

9. The assembly structure recited in claim 1, wherein the fold line comprises a change in a property of the substrate along the fold line.

10. The assembly structure recited in claim **1**, wherein there are at least two fold lines on the substrate, providing at least three sections that fold over each other to produce at least two active memory devices.

11. The assembly structure in Claim **10** wherein the three sections includes a center section having a set of conductor lines on both sides of the center section substrate to align with memory devices on both sides of the center section substrate after folding.

12. An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of memory material disposed on a first section of the multiple sections, of the memory device;

a second layer of memory material disposed on a second section of the multiple sections;

at least one fold line disposed on the substrate to define alignment of the memory materials on the first and second sections; wherein the sections may be folded on each other at the fold line to form an operable electronic device in the memory device.

13. The assembly structure of claim **12** wherein the memory materials on the first section comprise a first plurality of conductor lines and the memory materials on the second section comprise a second plurality of conductor lines, and wherein at least one of the memory materials comprise semiconductor materials.

14. The assembly structure of claim **13** wherein the memory materials of the first and second sections are fabricated so that, with the first and second sections folded on each other at the fold line, the first and second pluralities of conductor lines and the semiconductor materials are aligned with each other to form the operable electronic device in the memory device.

15. The assembly structure recited in claim **13**, wherein the first plurality of conductors are formed with an array of parallel conductors or wires spaced across the first section, and the second plurality of conductors section are formed with an array of parallel conductors or wires spaced across the second section, the

plurality of conductors on the second section being perpendicular to the plurality of conductors on the first section.

16. The assembly structure recited in claim **13** wherein the first and second sections are folded along the fold line so that the layers of memory material are in contact with each other, and wherein at least one of the first and second sections has semiconductor materials and patterns thereon to form a matrix of memory cells.

17. The assembly structure recited in Claim **13** wherein the conductors of the first section are fabricated with narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

18. The assembly structure recited in Claim **17**, wherein the conductors in the second section includes narrowing cross-section areas configured to align with the narrowing cross-section areas of the first section.

19. A method of fabricating multiple layers of a memory device, comprising:

assembling a common substrate having multiple sections;

constructing at least one fold line on the substrate to separate the multiple sections;

fabricating memory structure on at least two sections of the substrate; and

folding the substrate along the fold line to stack the multiple sections on top of each other and align the memory structures on adjacent folded sections to form at least one operable electrical device.

20. The method of fabricating multiple layers of a memory device recited in claim **19**, wherein the method comprises assembling a substrate having a fold line to form two sections.

21. The method of fabricating multiple layers of a memory device recited in claim **19**, wherein the memory structure on at least one section further comprises fabricating diode fuse patterns on at least one of the two sections, and aligning the two sections so that the diode fuse patterns coincide to form a matrix of diode fuses.

22. The method of fabricating multiple layers of a memory device recited in claim **20** wherein the memory structure on the two sections are fabricated to include conductor grids, the grids on the first section being perpendicular to the grids on the second section.

23. The method of fabricating multiple layers of a memory device recited in claim **22**, wherein the conductor grids of at least one of the first and second sections include conductors that vary in cross-section area at selected points on the conductors.

24. The method of fabricating multiple layers of a memory device recited in claim **19**, wherein the fold line is fabricated by applying multiple aligned perforations.

25. The method of fabricating multiple layers of a memory device recited in claim **19**, wherein at least two fold lines are fabricated on the substrate to provide at least three separate sections capable of folding to a stacked layer configuration.

26. The method of fabricating multiple layers of a memory device recited in claim **25**, wherein the sections are folded so that a center section on the substrate becomes a center layer of the folded sections.

27. The method of fabricating multiple layers of a memory device recited in claim **25**, wherein the sections are folded so that one of the end sections on the substrate becomes a center layer of the folded sections.

28. The method of fabricating multiple layers of a memory device recited in Claim **25** wherein the at least two fold lines are parallel with each other.

29. The method of fabricating multiple layers of a memory device recited in Claim **25** wherein the at least two fold lines are not parallel with each other.